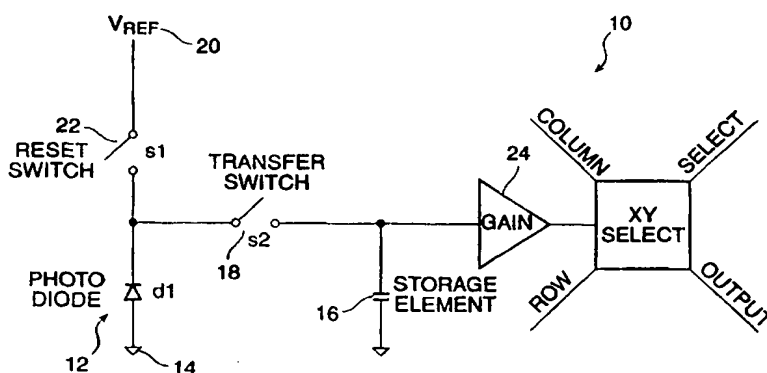




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(54) Title: INTRA-PIXEL FRAME STORAGE ELEMENT, ARRAY, AND ELECTRONIC SHUTTER METHOD SUITABLE FOR ELECTRONIC STILL CAMERA APPLICATIONS

**(57) Abstract**

A storage pixel sensor disposed on a semiconductor substrate comprises a capacitive storage element having a first terminal connected to a fixed potential and a second terminal. A photodiode has an anode connected to a first potential and a cathode. A semiconductor reset switch has a first terminal connected to the cathode and a second terminal connected to a reset potential. A semiconductor transfer switch has a first terminal connected to the cathode and a second terminal connected to the second terminal of the capacitive storage element. A semiconductor amplifier has an input connected to the capacitive storage element and an output. The semiconductor reset switch and the semiconductor transfer switch each has a control element connected to a control circuit for selectively activating the semiconductor reset switch and the semiconductor transfer switch. A light shield is disposed over portions of the semiconductor substrate comprising a circuit node including the second terminal of the semiconductor transfer switch, the second terminal of the capacitive storage element and the input of the semiconductor amplifier and to prevent substantially all photons from entering the circuit node. Structures are present for preventing substantially all minority carriers generated in the semiconductor substrate from entering the circuit node. A plurality of storage pixel sensors are disposed in an array.

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SPECIFICATIONINTRA-PIXEL FRAME STORAGE ELEMENT, ARRAY,
AND ELECTRONIC SHUTTER METHOD SUITABLE
FOR ELECTRONIC STILL CAMERA APPLICATIONS

20 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to image sensor arrays. More particularly, the present invention relates to CMOS image sensor arrays for still camera applications and to methods for operating those arrays.

25 2. The Prior Art

Integrated image sensors are known in the art. Such sensors have been fabricated from charge-coupled devices (CCDs) and as bipolar and MOS image sensors.

In the CCD imager art, on-chip frame storage capability has been employed previously. It has been motivated by the need to shift sensed charges out during a video frame time without
30 letting them be contaminated by further exposure as the charges travel across the CCD array. Two storage techniques are commonly employed in the CCD imager art. According to the first technique, a second separate on-chip CCD array is provided under a light shield, and the entire image is quickly shifted along one dimension into the storage array, since shifting in one dimension is fast enough to avoid significant contamination. According to the second technique,
35 line-storage CCDs are provided between the lines of sensors, with local light shielding. In the CCD art, techniques have been developed for preventing leakage and contamination due to minority carrier diffusion and leakage, but these techniques are not applicable to the CMOS sensor array because the silicon fabrication processes are different.

In still-camera applications with randomly-addressable CMOS active-pixel sensors, the
40 problem of how to implement a short-exposure interval with a long readout interval exists. A typical active-pixel area-array image sensor is disclosed in Hurwitz et al., "An 800K-Pixel Color CMOS Sensor For Consumer Still Cameras", SPIE Vol. 3019, pp 115-124 and comprises a plurality of rows and columns of pixel sensors. The most common method of exposure for this type of sensor array is to cyclicly scroll through the rows so that the integration duration for each
45 row is the same, but can be shorter than the total readout interval. This method of exposure

control is known as an electronic shutter.

There are two problems with this type of electronic shutter. First, since each row scans a different time interval, there will be motion artifacts (the shape of moving objects will be distorted). In addition, this scheme requires a very high conversion rate analog-to-digital converter (ADC) implementation. For example, if the array has 1 million pixels, and the readout duration is 1/100 sec (about the maximum acceptable for a hand-held camera), the required conversion rate is 100 million samples/sec. Since the state of the art for commercial ADCs with the required accuracy (10 bits) is about 20 million samples/sec, this means that a total of 5 ADCs would have to be used to allow for 1/100 sec exposures.

Another solution to the exposure problem is to provide a mechanical shutter for the camera. In this mode of operation, the entire array is first reset simultaneously. Then the shutter is opened for the duration of the exposure. After the shutter is closed, readout can take place at a relatively slow rate limited only by the dark current error in the pixels. However mechanical shutters add to the cost and complexity of the camera, and also contribute to camera shake.

Prior art in CMOS storage pixels has not yet addressed the problem of leakage and contamination, even though the problem has been noted. In the paper Yadid-Pecht et al., "A Random Access Photodiode Array for Intelligent Image Capture", IEEE Trans. Electron Devices vol. 38 no. 8 Aug. 1991 pp 1772-1779, a prior-art storage pixel is described. The imager disclosed therein is motivated by the need to access pixel values in random order for certain processing functions, as opposed to being motivated by the need to have a readout interval longer than the exposure interval in high resolution still photography. Yadid-Pecht et al. describe the problems of "crosstalk" and "leakage" being "much stronger than predicted," but they do not offer any specific ideas on how to ameliorate these problems.

The pixel layout in this prior-art imager shows that the authors did not find a strategy for protecting the sensitive storage node from stray carrier diffusion, nor from light. They reference three papers from the CCD art for "technological solutions" to these problems, but the CCD art referenced does not obviously apply to the problem of CMOS storage pixels.

It is therefore an object of the present invention to provide a pixel sensor and an array of pixel sensors which overcome some of the shortcomings of the prior art.

A further object of the present invention is to provide a storage-pixel sensor and an imaging array of storage-pixel sensors which overcomes the scanout problems inherent in prior-art imaging

arrays.

Another object of the present invention is to provide an improved electronic shutter method for use with storage-pixel sensors.

Yet another object of the present invention is to provide a storage-pixel sensor and an
5 imaging array of storage-pixel sensors which are compatible with the electronic shutter method of the present invention.

BRIEF DESCRIPTION OF THE INVENTION

According to one aspect of the present invention, a storage-pixel sensor and an array of
10 storage-pixel sensors suitable for use in an active-pixel area-array image sensor employing an electronic shutter method are disclosed.

According to a second aspect of the present invention, a method for implementing an electronic shutter having a greatly reduced ADC sample rate requirement is disclosed. The electronic shutter mechanism of the present invention has fewer motion artifacts than prior-art electronic shutter implementations.

15 BRIEF DESCRIPTION OF THE DRAWING FIGURES

FIG. 1 is a block diagram of a typical prior-art active-pixel area-array image sensor.

FIG. 2 is a timing diagram showing the common method of exposure for the type of sensor array of FIG. 1 comprising scrolling through the rows so that the integration duration for each row is the same.

20 FIG. 3a is a simplified schematic diagram of a storage-pixel sensor according to the present invention.

FIG. 3b is a timing diagram showing the exposure method according to the present invention.

25 FIG. 4 is a simplified schematic diagram of a correlated-double-sampling circuit which may be used with the storage-pixel sensor of FIG. 3a.

FIG. 5 is a block diagram of an image array making use of the storage technique of the present invention.

FIG. 6 is a schematic diagram of an NMOS-switch implementation of the storage-pixel sensor circuit of FIG. 3a.

FIGS. 7a and 7b are layout and cross sectional views, respectively, of the NMOS-switch implementation of the storage-pixel sensor circuit of FIG. 6.

5 FIG. 8 is a schematic diagram of a PMOS-switch implementation of the storage-pixel sensor circuit of FIG. 3a.

FIGS. 9a and 9b are layout and cross sectional views, respectively, of the PMOS switch implementation of the storage-pixel sensor circuit of FIG. 8.

10 FIGS. 10a and 10b are, respectively, a more detailed timing diagram of control signals and a schematic diagram of illustrative circuitry for operating an array of storage-pixel sensor arrays according to the present invention.

FIG. 11 is a magnified portion of portions of waveforms like those appearing in FIG. 10a, showing in more detail the voltage levels provided by level-shifter circuits for the various control signals used by the array of the present invention.

15 DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

20 To facilitate an understanding of the present invention, an understanding of the operation of prior-art active-pixel area-array image sensors is helpful. Referring first to FIG. 1, a block diagram of a typical prior-art active-pixel area-array image sensor is presented. A pixel array comprises m rows each having n columns of pixel elements.

25 A row-select circuit (shown at the left side of the array) is provided to scroll through the rows so that the integration duration for each row is the same. For each row, the analog value out of each pixel is multiplexed to ADC circuits to digitize the output values and provide a stream of digital data representing the outputs of the pixels in that row.

Referring now to FIG. 2, a timing diagram shows the common method of exposure for the type of sensor array of FIG. 1. As can be seen from an examination of FIG. 2, the row-select circuits scroll through the rows one at a time so that the integration duration for each row is the

same. The time interval between the scanning of the pixels in the first row and the scanning of pixels in the last row of the array of FIG. 1 can be considerable for large arrays, producing undesirable motion artifacts. Motion artifacts can, up to a point, be minimized by increasing the scanning rate of the sensor electronics comprising the multiplexers and ADC circuits, but for larger
5 arrays the increase in scanning speed is limited by the capabilities of the multiplexer and ADC circuits.

Referring now to FIG. 3a, a simplified schematic diagram of a storage-pixel sensor 10 suitable for use in the electronic shutter exposure method of the present invention is shown. Storage-pixel sensor 10 comprises a photodiode 12 having its anode connected to a fixed voltage potential 14 (shown in FIG. 3a as ground). The cathode of photodiode 12 is connectable to a
10 storage capacitor 16 via a transfer switch 18. Storage capacitor 16 has a first plate connected to transfer switch 18 and a second plate connected to a fixed potential (shown as ground 14 in FIG. 3a). The cathode of photodiode 12 is also connectable to a reference potential V_{ref} 20 via a reset switch 22 so that the photodiode 12 is reverse biased. An amplifier 24 has its input connected to
15 storage capacitor 16.

FIG. 3b is a timing diagram showing the operation of reset switch 22 (upper trace 30) and transfer switch 18 (lower trace 32). Referring now to both FIGS. 3a and 3b together, the operation of storage-pixel sensor 10 may be readily understood.

First, the pixel 10 is reset by turning on both reset switch 22 and transfer switch 18 as
20 shown by the high level of both reset-switch and transfer-switch traces 30 and 32 of FIG. 3b. Then the reset switch 22 is turned off at falling edge 34 of reset-switch trace 30 so that integration of photocurrent from photodiode 12 can begin. The photocurrent integration period is indicated by arrow 36.

When transfer switch 18 is turned on, the capacitance of the storage capacitor 16 adds to
25 the capacitance of the photodiode 12 during integration, thereby increasing the charge capacity and therefore dynamic range of the storage-pixel sensor. This also reduces variation in the pixel output due to capacitance fluctuations since gate oxide capacitance from which storage capacitor 16 is formed is better controlled than junction capacitance of the photodiode 12.

When the integration is complete (determined by external exposure control), the transfer
30 switch turns off at falling edge 38 of transfer-switch trace 32 of FIG. 3b, isolating the voltage level corresponding to the integrated photocharge onto the storage capacitor 16. Shortly thereafter, the photodiode 12 itself is reset to the reference voltage 20 by again turning on reset switch 24 as indicated by rising edge 40 of upper trace 30 of FIG. 3b. This action will prevent the photodiode

12 from continuing to integrate during the readout process and possibly overflowing excess charge into the substrate which could effect the integrity of the signal on the storage element.

After the reset switch 24 is turned back on, the readout process can begin. The readout period available for reading out all of the storage-pixel sensors in all rows is indicated at arrow 42 of FIG. 3b. As presently preferred, the pixel data value readout is performed using correlated double sampling.

FIG. 4 is a simplified schematic diagram of a correlated double sampling (CDS) circuit 50 which may be used with the storage-pixel sensor of FIG. 3a. CDS circuit 50 comprises an amplifier 52 employing input capacitor 54 having a first plate comprising an input node to the circuit and a second plate connected to the input of amplifier 52. A switch 56 is disposed between the input of amplifier 52 and a fixed reference potential shown as ground in FIG. 4.

The operation of the CDS circuit of FIG. 4 may be understood from the following explanation. First, the signal level for each pixel is read out and stored in the sampling circuitry in the column, controlled by pulse 58 controlling switch 56, as shown in figure 4. Then transfer switch 18 is turned on again (for that row only, as seen by rising edge 44 of transfer-switch trace 32 of FIG. 3b) which makes the reference level available to the sampling circuit. This form of double sampling allows for canceling of noise sources in the pixel and column that are slowly varying compared to the time between the two samples.

With the first signal voltage (V_1) present on the left of the capacitor 54, switch 56 is on. The voltage stored across capacitor 54 is equal to the signal voltage V_1 . Then switch 56 is turned off, and the voltage on the first plate of capacitor 54 moves to a new level (V_2) representing the reference voltage. The voltage across capacitor 54 will not change during this time because there is negligible current flowing into the amplifier 52 or through switch 56. Thus both plates of capacitor 54 will change by $(V_2 - V_1)$, and the voltage at the input of amplifier 52 at the end of the cycle will be $(V_2 - V_1)$. In this way, noise, offsets, etc can be subtracted from the output of the array.

With the sampling scheme described above, the difference output at the output of amplifier 52 will contain noise from the reset switch 22 of FIG. 3a because the signal contains the reset noise but the reference voltage does not. However, this noise should be fairly repeatable and therefore easily canceled in the post processing environment. There will also be signal dependent charge injection from the transfer switch 18. However this source of noise can be considered a non-linearity in the system, one of many non-linearities including the pixel amplifier gain deviation and the variation of the photodiode capacitance with voltage.

Persons of ordinary skill in the art will recognize that the CDS circuit disclosed in FIG. 4 herein is merely exemplary and that other CDS circuits may be employed in the present invention. For example, the CDS circuit disclosed in co-pending application serial No. 08/867,472, filed June 2, 1997, may also be used as can other equivalent CDS circuits.

5 Embodiments of the present invention which do not employ correlated double sampling are also contemplated herein. In such embodiments, rising edge 44 of transfer-switch trace 32 of FIG. 3b is not needed and transfer-switch trace 32 stays low until the all of the rows have been read out or another cycle is initiated.

10 Referring now to FIG. 5, a block diagram of an active-pixel imaging array 60 employing the storage technique of the present invention is shown. Like the image array of FIG. 1, image array 60 may comprise an m row by n column array 62 of active-pixel elements. Unlike the array of FIG. 1, each storage-pixel sensor element of the array of FIG. 5 is an element like that of FIG. 3a.

15 A row decoder circuit 64 is used to select rows of the array. Row decoder circuits, such as row address decoder circuits are well known in the art. Row-select pulse 66 and transfer gate pulse 68 are ANDed with the decoded row address signal in row decoder 64 to produce the timing signals shown in FIG. 3b for each row.

20 Row decoder circuit 64, along with column sampling circuits and multiplexer 70 are used to extract the pixel information from the array and present it to ADC circuit 72 for digitizing. The column sampling circuits used in array 60 may comprise a decoder similar to the row decoder circuit 64 and column sampling circuit 70 may be driven from a counter 74. Techniques for using counters to drive row and column decoding circuitry are known in the art. Typically, the higher-order bits from counter 74 are used to drive the row decoder circuit 64 and the lower-order bits are used to drive column sampling circuit and multiplexer 70 to permit extraction of all pixel
25 information in a row of the array prior to selection of the next row by row decoder circuit 64.

30 Because the storage technique of the present invention affords a substantial increase in the time available to read individual pixel values out of the array, use of a single ADC circuit 72 is made possible in active-pixel imaging array 60. As will be appreciated by persons of ordinary skill in the art, a higher-resolution ADC circuit 72 (e.g., 12 bits) may be employed in the imager of the present invention at lower power than ADC circuits that are operating near their performance limit in prior-art imagers.

The length of time available for the readout process is limited by leakage onto the node of the transfer switch that is connected to the storage capacitor 16 of FIG. 3a. This leakage can be either dark (generation/diffusion) current or photo current. Measured dark current for a sub half micron process is about 100 electrons/sec/ μm^2 at room temperature. Since the diffusion area for the transistor devices in the pixels can be made as small as $1 \mu\text{m}^2$, this implies 100 electrons/sec leakage current, which amounts to a 0.2 mV error in the stored signal over 1 second in an embodiment where storage capacitor 16 has a value of 80 fF ($5 \text{ fF}/\mu\text{m}^2 \times 16 \mu\text{m}^2$). This represents a small source of error yet extends the read time for the array by a factor of 100 compared to prior art arrays.

If the storage pixel is used in conjunction with a mechanical shutter, the read time limited by dark current can be extended proportional to the ratio of the photodiode area to the transfer switch diffusion area (about 20:1) relative to a simple non-storage pixel used with a mechanical shutter.

The dominant source of error in the storage pixel of the array of the present invention is collection of stray photocurrent in the form of minority carriers. According to another aspect of the present invention, the structure of the storage-pixel sensor of the present invention is chosen to minimize stray photocurrent leakage. FIGS. 6, 7a and 7b, 8, and 9a and 9b, to which attention is now drawn, show cross sections and layout details associated with NMOS and PMOS implementations of the schematic of FIG. 3a that primarily address the stray photocurrent leakage issue.

Referring now to FIG. 6, a schematic diagram of an NMOS embodiment of the storage-pixel sensor is shown. All transistors are NMOS, and the photodiode is n+/p-. Although an n+/p-well photodiode is shown, the method would also work with a p+/n-well photodiode.

NMOS storage-pixel sensor 80 employs photodiode 82 having its anode grounded and its cathode connected to the source of N-Channel MOS reset transistor 84. The drain of N-Channel MOS reset transistor 84 is connected to V_{ref} and its gate is connected to the reset line (reference numeral 76 of FIG. 5) which is common to all pixels in the array. The reset line is driven to a voltage at least a threshold above V_{ref} to ensure that the pixels are reset fully to the potential V_{ref} .

In the embodiment of FIG. 6, storage capacitor 16 of FIG. 3a is implemented as an N-Channel MOS storage capacitor transistor 86 with its source and drain tied to ground. N-Channel MOS storage capacitor transistor 86 is coupled to the cathode output of photodiode 82 through N-Channel MOS transfer transistor 88. The gate of N-Channel MOS transfer transistor 88 is connected to transfer line 90.

The voltage on the gate of N-Channel MOS storage capacitor transistor 86 is sensed by N-Channel MOS output transistor 92. N-Channel MOS output transistor 92 operates in source-follower mode, having its drain connected to Vcc and its source connected to N-Channel MOS select transistor 94. According to a presently- contemplated embodiment of the storage-pixel sensor 80 of the present invention, the voltage potential $V_{cc} = V_{ref}$. The gate of N-Channel MOS select transistor 94 is driven by select line 96.

Transfer line 90 and select line 96 are driven from a transfer gate pulse on transfer gate line 68 and a row-select pulse on row-select line 66, respectively, of FIG. 5. Both of these signals are gated by a row address decode signal from row decoder 64 of FIG. 5 to assure that only the pixels in a selected row are affected. The transfer gate pulse can also be ON to all rows simultaneously during reset.

N-Channel MOS storage capacitor transistor 86 will have the full gate oxide capacitance to the inversion layer under its gate as long as the voltage on the storage node is $> V_{TN}$ (about 0.6V). The pixel output will not be linear unless the voltage on the storage node is $> V_{TN}$ otherwise the source follower output transistor will be not turned on. Note that the bottom plate of the capacitor is tied to substrate (0 volts) through a butted p+/n+ contact, to eliminate the need for a separate ground wire in the array.

Referring now to FIGS. 7a and 7b, top and cross-sectional views, respectively of a presently preferred layout of the NMOS storage-pixel sensor 80 of FIG. 6, an important aspect of the invention will be illustrated. The cross section of FIG. 7b is taken through the arrow marked 7b-7b in FIG. 7a.

NMOS storage-pixel sensor 80 is fabricated on a p-type substrate 110. Field oxide regions 112 and 114 separate the active regions of the pixel from one another and field oxide regions 116 and 118 separate the storage-pixel sensor 80 from adjacent storage pixel sensors. Field oxide region 120 belongs to the nearest neighbor storage pixel sensor to the right of storage-pixel sensor 80.

Photodiode 82 of NMOS storage-pixel sensor 80 of FIG. 6 has n+ region 122 as its cathode and the p-substrate 110 as its anode. Storage capacitor 86 of FIG. 6 has polysilicon strip 124 as its upper plate and the p-substrate 110 as its lower plate. P-well 126 isolates the photodiode from the storage capacitor by making an electron-repelling barrier between the regions.

N-Channel MOS transistors 84, 88, 92, and 94 are all formed in p-well 128 and are all

easily seen in FIG. 7a, in which n+ region 130 is connected to polysilicon strip 124 of the storage capacitor via metal line 132 and forms drain of N-Channel MOS transfer transistor 88 of FIG. 6. N+ region 134 is connected to N+ cathode region 122 of the photodiode via metal line 136 and forms the source of both N-Channel MOS transistors 84 and 88 of FIG. 6. N+ region 138 is connected to Vcc metal line 140 and forms the drains of both N-Channel MOS reset transistor 84 and N-Channel MOS source-follower transistor 92 of FIG. 6. Persons of ordinary skill in the art will recognize that, in order to avoid overcomplicating the drawing figure and thus unnecessarily obscuring details of the invention, only a small portion of metal line 140 is shown as a square region surrounding the contact depicted in its center. Such skilled persons will appreciate that interconnections are made as disclosed herein in layers such as metal 2 or metal 3 layers of the integrated circuit containing this structure. Other metal lines are similarly depicted.

N+ region 142 forms the source of N-Channel MOS source-follower transistor 92 and the drain of N-Channel MOS select transistor 94. N+ region 144 forms the source of N-Channel MOS select transistor 94 and is connected to metal line 146 forming the column output line for the column of the array containing NMOS storage pixel sensor 80.

Polysilicon strip 148 comprises the gate of N-Channel MOS transfer transistor 88 and is connected to transfer metal line 150 common to all pixels in the row of the array containing pixel 80. Polysilicon strip 152 comprises the gate of N-Channel MOS reset transistor 84 and is connected to reset metal line 154, common to all pixels in the array. Polysilicon strip 156 extending from the polysilicon strip 124 forming the top plate of the storage capacitor comprises the gate of N-Channel MOS source-follower transistor 92. Polysilicon strip 158 comprises the gate of N-Channel MOS select transistor 96 and is connected to select metal line 160, common to all pixels in the column of the array containing the pixel 80.

Metal region 162 (shown in FIG. 7b) is disposed over the structure of the storage pixel 80 and serves as a light shield to prevent photocurrent generation in all regions of storage pixel 80 except the photodiode disposed under aperture 164 formed therein.

An important feature of the layout of NMOS storage-pixel sensor 80 is shown in the figures. In a typical CMOS process the p-well mask is generated as a reverse field of the n-well mask. However since the p-well and n-well implants are masked separately for sub 0.5 um processes, there is no reason why the p-well and n-well must be complementary layers. According to this aspect of the present invention this fact is used advantageously. As shown in FIGS. 7a and 7b, the p-well 128 is placed under all of the N-Channel MOS transistors, and the p-well 126 is placed between the capacitor bottom plate and the photodiode (in this latter case for isolation). Elsewhere there is no p-well or n-well either, only the doping level from the starting

wafer (about $1E15$ p-type). Furthermore the metal line 162 comprising the light shield extends out over the edges of the p-well 128. This means that photocurrent will only be generated outside the p-well 128 in the bulk.

Since the p-well 128 is doped 100 times more heavily than the p-substrate ($10E17$ vs. $10E15$), there is a potential barrier for electrons to enter the p-well from the bulk of about 100 mV as shown diagrammatically at reference numerals 166. This will suppress collection of electron current by n+ diffusions inside the p-well by about 100 times (using the diode rule of thumb 62 mV/decade of current). Photocurrent generated outside the p-well will be preferentially collected by the n+ region 168 of the photodiode of the adjacent pixel (biased to 5V during the readout interval) or the adjacent capacitor bottom plate shown at reference numeral 170 (at zero volts but still a potential well for electrons).

It should perhaps also be noted that the n+ diffusion 130 connected to the upper plate of the storage capacitor is adjacent within the p-well to the photodiode node on one side (n+ region 134), and the output node (n+ region 144 of the adjacent pixel) on the other side. Both of these diffusions will be biased positively and therefore will collect electron current within the p-well that would otherwise end up on the storage node 130. It is again emphasized that the light shield covers the entire p-well which minimizes photo generated minority carriers within the p-well.

Referring now to FIG. 8, a schematic diagram of an alternate embodiment of a storage pixel sensor 180 according to the present invention is shown utilizing P-Channel reset and transfer transistors. Storage pixel sensor 180 employs photodiode 182 having its anode grounded and its cathode connected to the drain of P-Channel MOS reset transistor 184. The source of P-Channel MOS reset transistor 184 is connected to Vcc and its gate is connected to the reset line (reference numeral 76 of FIG. 5) which is common to all storage pixel sensors in the array.

As in the embodiment of FIG. 6, storage capacitor 16 of FIG. 3a is implemented in the storage pixel sensor of FIG. 8 as an N-Channel MOS storage capacitor transistor 186 with its source and drain tied to ground. N-Channel MOS storage capacitor transistor 186 is coupled to the cathode output of photodiode 182 through P-Channel MOS transfer transistor 188. The gate of P-Channel MOS transfer transistor 188 is connected to transfer line 190.

The voltage on the gate of N-Channel MOS storage capacitor transistor 186 is sensed by N-Channel MOS output transistor 192. N-Channel MOS output transistor 192 operates in source-follower mode, having its drain connected to Vcc and its source connected to N-Channel MOS select transistor 194. According to a presently- contemplated embodiment of the storage pixel sensor 180 of the present invention, the voltage potential $V_{cc} = V_{ref}$. The gate of N-Channel

MOS select transistor 194 is driven by select line 196.

As in the embodiment of FIG. 6, the transfer line 190 and select line 196 of storage pixel 180 of FIG. 8 are driven from a transfer gate pulse on transfer gate line 68 and a row-select pulse on row-select line 66, respectively, of FIG. 5. Both of these signals are gated by a row address
5 decode signal from row decoder 64 of FIG. 5 to assure that only the pixels in a selected row are affected.

The P-Channel MOS reset transistor 184 is used to reset the photodiode all the way to the positive rail, which would not be possible using the N-Channel MOS reset transistor 84 of the embodiment of FIG. 6. The photodiode 182 still comprises an n+/p junction since that type of
10 photodiode is known to have lower leakage than p+/n-. The source follower output transistor 192 of the embodiment of FIG. 8 remains an N-Channel device since a P-Channel MOS source follower transistor would not be active with its gate near the positive supply rail.

The select transistor 194 is also an N-Channel device since the signal to be passed out of the pixel is always less than $V_{cc} - V_t$. The storage capacitor 186 is formed as an N-Channel
15 transistor for the same reasons and in the same way as described for the pixel 80 of FIG. 6.

One issue of concern with respect to the P-Channel MOS transistors of the embodiment of FIG. 8 is subthreshold current. In the embodiment of FIG. 6 employing only N-Channel devices, the useful voltage swing on the circuit node comprising the upper polysilicon plate of storage capacitor 86 is V_{ref} to V_{TN} wherein the leakage is dominated by the junctions and is about
20 $0.02fA/\mu m^2$ of junction area. In the embodiment of FIG. 8, the leakage is dominated by P-Channel subthreshold current, and is about $10pA/\mu m$ of device width if $V_{cc}=V_{ref}$. This value is reduced by a factor of 10 for every 80mv that the reset high logic level (typically V_{cc}) exceeds V_{ref} . V_{ref} should be decreased about 0.50V to reduce the order of junction leakage. Reducing the reference voltage in the array does, however, reduce the increase in pixel output swing.

Referring now to FIGS. 9a and 9b, top and cross sectional views of a presently preferred
25 layout of the pixel of FIG. 8 are presented. The cross section of FIG. 9b is taken through the arrow marked 9b-9b in FIG. 9a.

Like the NMOS storage pixel sensor 80 of FIG. 6, storage pixel sensor 180 of FIG. 8 is fabricated on a p-type substrate 200. Field oxide regions 202 and 204 separate the active regions
30 of the pixel from one another and field oxide regions 206 and 208 separate the storage pixel sensor from adjacent storage pixel sensors. Field oxide region 210 belongs to the nearest neighbor storage pixel sensor to the right of pixel 180. A topological difference between the layout of pixel

80 as seen in FIGS. 7a and 7b and the layout of storage pixel sensor 180 of FIGS. 9a and 9b is that the storage capacitor in pixel 180 of FIGS. 9a and 9b is disposed at the right-hand side of the storage pixel sensor rather than in the center. This is a design detail which is not crucial to the invention.

5 Photodiode 182 of NMOS storage pixel sensor 180 of FIG. 8 has n+ region 212 as its cathode and p-well region 214 as its anode. Storage capacitor 186 of FIG. 8 has polysilicon strip 216 as its upper plate and p-well region 218 as its lower plate. Those of ordinary skill in the art will appreciate that p-well regions 214 and 218 can be part of the same p-well.

10 P-Channel MOS transistors 184 and 188 are formed in n-well 220 and are easily seen in FIG. 9a, in which p+ region 222 is connected to polysilicon strip 216 of the storage capacitor via metal line 224 and forms the source of P-Channel MOS transfer transistor 188 of FIG. 8. P+ region 226 is connected to n+ cathode region 212 of the photodiode via metal line 228 and forms both the drain of P-Channel MOS transfer transistor 188 and the drain of P-Channel MOS reset transistor 184 of FIG. 8. P+ region 230 is connected to Vcc metal line 232 and forms the source of P-Channel MOS reset transistor 184. Metal line 232 also bridges the border of n-well 220 to connect p+ region 230 in the n-well 220 to n+ region 234 which forms the drain of N-Channel MOS source-follower transistor 192 of FIG. 8. N+ region 236 forms the source of N-Channel MOS source-follower transistor 192 and the drain of N-Channel MOS select transistor 194. N+ region 238 forms the source of N-Channel MOS select transistor 194 and is connected to metal line 240 forming the column output line for the column of the array containing storage pixel 180.

25 Polysilicon strip 242 comprises the gate of P-Channel MOS transfer transistor 188 and is connected to transfer metal line 244, common to all storage pixel sensors in the row containing storage pixel sensor 180. Polysilicon strip 246 comprises the gate of P-Channel MOS reset transistor 184 and is connected to reset metal line 248, common to all storage pixel sensors in the array. Polysilicon strip 250 extending from the polysilicon strip 216 forming the top plate of the storage capacitor comprises the gate of N-Channel MOS source-follower transistor 192. Polysilicon strip 252 comprises the gate of N-Channel MOS select transistor 196 and is connected to select metal line 254, common to all storage pixel sensors in the column containing storage pixel sensor 180.

30 Metal line 256 is disposed over the n-well 220 and over the n+ diffusions for transistors 192 and 194 and serves as a light shield to minimize the concentration of photo generated minority carriers (holes) within the well which could contribute to leakage of the storage node. Apertures 258 allow light to enter in the region of the photodiode of storage pixel 180 indicated at n+region 212 and n+region 260 of the photodiode of the adjacent storage pixel. The pixel 180 of FIGS. 8,

9a. and 9b is 50% larger than pixel 80 of FIGS. 6, 7a. and 7b. however it should provide a longer readout duration than the pixel 80 and a larger output voltage swing as well.

The storage pixels of the present invention differ in several respects from prior-art pixels which provide for storage. The present invention uses a different circuit with fewer transistors and control lines, and uses a different timing scheme, which allows a higher dynamic range of charge integration, and allows for relatively longer frame storage times as needed in high resolution still photography, all these features being enabled by the improved leakage and contamination performance.

Referring now to FIGS. 10a and 10b, respectively, more detailed diagrams are presented of control signals and circuitry for operating an array of storage-pixel sensor arrays according to the present invention. FIGS. 10a and 10b illustrate the operation of the reset, transfer, and select signals used to operate an array as presently preferred according to the present invention. Persons of ordinary skill in the art will appreciate that control circuitry 272 depicted in FIG. 10b is illustrative only and that other configurations may be employed to generate the waveforms shown in FIG. 10a.

Referring now to both FIGS. 10a and 10b, several control signal waveform traces are presented. The first waveform of FIG. 10a represents Global Transfer control signal 270. This control signal is shown at the left side of the control circuitry 272 depicted in FIG. 10b as appearing on line 274. Control circuitry 272 may be disposed in or associated with Row decoder 64 of FIG. 2.

The second waveform of FIG. 10a represents Reset control signal 276. This control signal is generated by the control circuitry of FIG. 10b and appears on line 278.

The third waveform of FIG. 10a represents Row N Select control signal 280. The Row N Select control signal is derived from decoder gate 282 in control circuitry 272 using the appropriate Row N address bits and their complements as is well known in the art. The Row N Select control signal appears on line 284.

The fourth waveform of FIG. 10a is the CDS Clock signal 286. CDS Clock signal 286 is shown on only a portion of the horizontal direction representing the time axis in FIG. 10a in order to avoid unnecessarily complicating the drawing figure. CDS Clock signal 286 is shown at the left side of the control circuitry 272 depicted in FIG. 10b as appearing on line 288.

The last waveform of FIG. 10a is the Row N Transfer control signal 290. Row N

Transfer control signal 290 is an output of the control circuitry 272 appearing on line 292 of FIG. 10b.

Turning to FIG. 10b in more detail, the Row N Select signal on line 284 is combined with the CDS Clock signal on line 288 and the Global Transfer signal on line 274 through inverter 294, AND gate 296, OR gate 298, and level-shifter circuit 300 to produce Row N Transfer signal 290 on line 292. Global Transfer signal on line 274 is presented to delay circuit 302, inverter 304, and level-shifter circuit 306 to produce Reset signal on line 278.

Level-shifter circuits 300 and 306 are used to provide sufficient high and low voltage levels for the Row N Transfer signal 290 and Reset signal 276 to assure full reset, low leakage, overflow drainage, etc., and to generally optimize the operation of the array. This is explained diagrammatically in FIG. 11.

The CDS Clock signal on line 288 is also presented to the CDS circuit illustrated in the lower left hand portion of FIG. 10b. The CDS circuit is shown configured in and operates as described with reference to FIG. 4. Thus CDS Clock signal on line 288 turns on N-Channel MOS transistor 308 which functions as switch 56 in FIG. 4. Capacitor 54 is also shown in FIG. 4 as driving amplifier 52 from column line 310. N-Channel bias transistor 312, its gate connected to bias voltage V_{bias} , maintains a bias current flow of magnitude i as shown. Typical values for the bias voltage and current are about 1 volt and about 5 μA .

In embodiments of the present invention that do not employ correlated double sampling, inverter 294, AND gate 296, and OR gate 298 are not used, and the global transfer signal on line 274 is connected directly to the input of a single level shifter circuit to drive all transfer switches in the array.

Referring now to FIG. 11, it may be seen that the voltage levels of the signals used to drive the gates of transfer switch 18 and reset switch 22 of FIG. 3a should be sufficient to fully turn on the MOS transistor switch devices such that no V_{th} drop appears across these devices. In addition, a raised low level value (e.g., about 1.5 volts) on the reset line allows electrons to overflow to V_{ref} during integration to prevent overflow from brightly-lighted pixels into adjacent pixels. Those of ordinary skill in the art will appreciate that the timing of the signals shown in FIG. 11 is arbitrary since the figure is meant to illustrate the voltage levels of the signals used to drive the gates of transfer switch 18 and reset switch 22 of FIG. 3a with reference to ground potential and V_{ref} . The Reset signal (trace 314) is shown having a high level above that of V_{ref} and a low level elevated above ground. The Transfer signal (trace 316) is shown having a high level above that of V_{ref} and a low level at about ground potential.

Those of ordinary skill in the art will readily appreciate that the semiconductor structures described herein could be fabricated on an n-type substrate instead of a p-type substrate by reversing all p and n regions shown in FIGS. 7a, 7b, 9a, and 9b. In addition, such skilled persons will realize that other type changes between p and n devices could be implemented without
5 departing from the teachings of the invention.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

What is claimed is:

1. A storage pixel sensor disposed on a semiconductor substrate comprising:
a capacitive storage element having a first terminal connected to a fixed potential
and a second terminal;
5 a photodiode having a first terminal connected to a first potential and a second
terminal;
a semiconductor reset switch having a first terminal connected to said second
terminal of said photodiode and a second terminal connected to a reset potential that reverse biases
said photodiode;
10 a semiconductor transfer switch having a first terminal connected to said second
terminal of said photodiode and a second terminal connected to said second terminal of said
capacitive storage element;
a semiconductor amplifier having an input connected to said second terminal of said
capacitive storage element and an output;
15 said semiconductor reset switch and said semiconductor transfer switch each
having a control element connected to a control circuit for selectively activating said semiconductor
reset switch and said semiconductor transfer switch;
a light shield disposed over portions of the semiconductor substrate comprising a
circuit node including said second terminal of said semiconductor transfer switch, said second
20 terminal of said capacitive storage element and said input of said semiconductor amplifier and to
prevent substantially all photons from entering said circuit node; and
minority carrier rejection means for preventing substantially all minority carriers
generated in said semiconductor substrate from entering said circuit node.

2. The storage pixel sensor of claim 1, further including a semiconductor select switch
25 having an input connected to the output of said amplifier, an output connected to an output bus,
and a control element connected to said control circuit.

3. The storage pixel sensor of claim 1 wherein:
said semiconductor substrate is formed from a semiconductor material of a first
conductivity type;

30 said light shield is a portion of a metal interconnect layer disposed over said
semiconductor substrate;

said semiconductor transfer switch comprises a MOS transistor of a second
conductivity type opposite said first conductivity type, said MOS transistor formed in a well of
said first conductivity type, said well disposed in said semiconductor substrate, wherein said
35 minority carrier rejection means comprises said well.

4. The storage pixel sensor of claim 1 wherein:
said semiconductor substrate is formed from a semiconductor material of a first conductivity type;

5 said light shield is a portion of a metal interconnect layer disposed over said semiconductor substrate;

said semiconductor transfer switch comprises a MOS transistor of said first conductivity type formed in a well of a second conductivity type opposite said first conductivity type, said well disposed in said semiconductor substrate, wherein said minority carrier rejection means comprises said well.

10 5. The storage pixel sensor of claim 1 wherein:

said semiconductor substrate is p-type semiconductor substrate;

said light shield is a portion of a metal interconnect layer disposed over said semiconductor substrate;

15 said semiconductor transfer switch comprises an N-Channel MOS transistor formed in a p-well formed in said p-type semiconductor substrate, wherein said minority carrier rejection means comprises said p-well.

6. The storage pixel sensor of claim 1 wherein:

said semiconductor substrate is p-type semiconductor substrate;

20 said light shield is a portion of a metal interconnect layer disposed over said semiconductor substrate;

said semiconductor transfer switch each comprise a P-Channel MOS transistor formed in an n-well formed in said p-type semiconductor substrate, wherein said minority carrier rejection means comprises said n-well.

25 7. An array of storage pixel sensors disposed on a semiconductor substrate, the array comprising:

a plurality of storage pixel sensors, each storage pixel sensor including:

a capacitive storage element having a first terminal connected to a fixed potential and a second terminal;

30 a photodiode having a first terminal connected to a first potential and a second terminal;

a semiconductor reset switch having a first terminal connected to said second terminal of said photodiode and a second terminal connected to a reset potential that reverse biases said photodiode;

35 a semiconductor transfer switch having a first

terminal connected to said second terminal of said photodiode and a second terminal connected to said second terminal of said capacitive storage element;

a semiconductor amplifier having an input connected to said second terminal of said capacitive storage element and an output;

said semiconductor reset switch and said semiconductor transfer switch each having a control element for selectively activating said semiconductor reset switch and said semiconductor transfer switch;

a light shield disposed over portions of the semiconductor substrate comprising a circuit node including said second terminal of said semiconductor transfer switch, said second terminal of said capacitive storage element and said input of said semiconductor amplifier and to prevent substantially all photons from entering said circuit node; and

minority carrier rejection means for preventing substantially all minority carriers generated in said semiconductor substrate from entering said circuit node;

means for generating a reset signal and for coupling said reset signal to the control elements of all reset switches in the array;

means for generating a global transfer signal and for coupling said global transfer signal to the control elements of all transfer switches in the array;

means for generating a row transfer signal for each row in the array and for coupling the row transfer signal for each row to the control elements of all transfer switches associated with that row; and

a column line for each column in the array, each column line coupled to the outputs of the ones of the semiconductor amplifier associated with that column.

8. The array of claim 7 wherein each storage pixel sensor further includes a semiconductor select switch having an input connected to the output of said amplifier, an output connected to an output bus, and a control element connected to said control circuit.

9. The array of claim 7 wherein:
said semiconductor substrate is formed from a semiconductor material of a first conductivity type;

said light shield in each storage pixel sensor is a portion of a metal interconnect layer disposed over said semiconductor substrate;

said semiconductor transfer switch in each storage pixel sensor comprises a MOS transistor of a second conductivity type opposite said first conductivity type, said MOS transistor formed in a well of said first conductivity type, said well disposed in said semiconductor substrate, wherein said minority carrier rejection means comprises said well.

5 10. The array of claim 7 wherein:

said semiconductor substrate is formed from a semiconductor material of a first conductivity type;

said light shield in each storage pixel sensor is a portion of a metal interconnect layer disposed over said semiconductor substrate;

10 said semiconductor transfer switch in each storage pixel sensor comprises a MOS transistor of said first conductivity type formed in a well of a second conductivity type opposite said first conductivity type, said well disposed in said semiconductor substrate, wherein said minority carrier rejection means comprises said well.

11. The array of claim 7 wherein:

15 said semiconductor substrate is p-type semiconductor substrate;

said light shield in each storage pixel sensor is a portion of a metal interconnect layer disposed over said semiconductor substrate;

20 said semiconductor transfer switch in each storage pixel sensor comprises an N-Channel MOS transistor formed in a p-well formed in said p-type semiconductor substrate, wherein said minority carrier rejection means comprises said p-well.

12. The array of claim 7 wherein:

said semiconductor substrate is p-type semiconductor substrate;

said light shield in each storage pixel sensor is a portion of a metal interconnect layer disposed over said semiconductor substrate;

25 said semiconductor transfer switch in each storage pixel sensor comprises a P-Channel MOS transistor formed in an n-well formed in said p-type semiconductor substrate, wherein said minority carrier rejection means comprises said n-well.

13. An array of storage pixel sensors disposed on a semiconductor substrate, the array comprising:

30 a plurality of storage pixel sensors, each storage pixel sensor including:

a capacitive storage element having a first terminal connected to a fixed potential and a second terminal;

a photodiode having a first terminal connected to a first potential and a second terminal;

a semiconductor reset switch having a first terminal connected to said second terminal of said photodiode and a second terminal connected to a reset potential that reverse biases said photodiode;

5 a semiconductor transfer switch having a first terminal connected to said second terminal of said photodiode and a second terminal connected to said second terminal of said capacitive storage element;

10 a semiconductor amplifier having an input connected to said second terminal of said capacitive storage element and an output;

said semiconductor reset switch and said semiconductor transfer switch each having a control element for selectively activating said semiconductor reset switch and said semiconductor transfer switch;

15 a light shield disposed over portions of the semiconductor substrate comprising a circuit node including said second terminal of said semiconductor transfer switch, said second terminal of said capacitive storage element and said input of said semiconductor amplifier and to prevent substantially all photons from entering said circuit node; and

20 minority carrier rejection means for preventing substantially all minority carriers generated in said semiconductor substrate from entering said circuit node;

25 means for generating a reset signal and for coupling said reset signal to the control elements of all reset switches in the array;

means for generating a transfer signal and for coupling said transfer signal to the control elements of all transfer switches in the array; and

30 a column line for each column in the array, each column line coupled to the outputs of the ones of the semiconductor amplifier associated with that column.

14. The array of claim 12 wherein each storage pixel sensor further includes a semiconductor select switch having an input connected to the output of said amplifier, an output connected to an output bus, and a control element connected to said control circuit.

15. The array of claim 12 wherein:
35 said semiconductor substrate is formed from a semiconductor material of a first conductivity type;

said light shield in each storage pixel sensor is a portion of a metal interconnect layer disposed over said semiconductor substrate;

said semiconductor transfer switch in each storage pixel sensor comprises a MOS transistor of a second conductivity type opposite said first conductivity type, said MOS transistor formed in a well of said first conductivity type, said well disposed in said semiconductor substrate, wherein said minority carrier rejection means comprises said well.

16. The array of claim 12 wherein:

said semiconductor substrate is formed from a semiconductor material of a first conductivity type:

said light shield in each storage pixel sensor is a portion of a metal interconnect layer disposed over said semiconductor substrate;

said semiconductor transfer switch in each storage pixel sensor comprises a MOS transistor of said first conductivity type formed in a well of a second conductivity type opposite said first conductivity type, said well disposed in said semiconductor substrate, wherein said minority carrier rejection means comprises said well.

17. The array of claim 12 wherein:

said semiconductor substrate is p-type semiconductor substrate:

said light shield in each storage pixel sensor is a portion of a metal interconnect layer disposed over said semiconductor substrate;

said semiconductor transfer switch in each storage pixel sensor comprises an N-Channel MOS transistor formed in a p-well formed in said p-type semiconductor substrate, wherein said minority carrier rejection means comprises said p-well.

18. The array of claim 12 wherein:

said semiconductor substrate is p-type semiconductor substrate:

said light shield in each storage pixel sensor is a portion of a metal interconnect layer disposed over said semiconductor substrate;

said semiconductor transfer switch in each storage pixel sensor comprises a P-Channel MOS transistor formed in an n-well formed in said p-type semiconductor substrate, wherein said minority carrier rejection means comprises said n-well.

19. A method for operating a storage pixel sensor of claim 1 including the steps of:

(1) turning on the transfer switch of the storage pixel sensor for a first time period and turning off said transfer switch at the end of said first time period;

(2) turning on the reset switch of the storage pixel sensor for a reset period

occurring during a first portion of said first time period and turning off said reset switch at the end of said first portion of said first time period:

(3) integrating photocurrent in the storage pixel sensor for an integration period occurring during a second portion of said first time period after said reset switch has been turned off, said integration period ending at the end of said first time period;

(4) turning on the reset switch of the storage pixel sensor after the end of said first time period; and

(5) reading an output signal from the amplifier of the storage pixel sensor.

20. A method for operating the storage pixel sensor of claim 1, including the steps of:

(1) turning on the transfer switch of the storage pixel sensor for a first time period and turning off said transfer switch at the end of said first time period;

(2) turning on the reset switch of the storage pixel sensor for a reset period occurring during a first portion of said first time period and turning off said reset switch at the end of said first portion of said first time period;

(3) integrating photocurrent in the storage pixel sensor for an integration period occurring during a second portion of said first time period after said reset switch has been turned off, said integration period ending at the end of said first time period;

(4) turning on the reset switch of the storage pixel sensor for a reference period after the end of said first time period; and

(5) reading an output signal from the storage pixel sensor, then activating the transfer switch of the storage pixel sensor and reading a reference signal from the storage pixel sensor, then taking the difference between the output signal and the reference signal for the storage pixel sensor.

21. A method for operating an array of storage pixel sensors of claim 1 arranged in rows, including the steps of:

(1) turning on the transfer switches of all storage pixel sensors in the array for a first time period and turning off said transfer switches at the end of said first time period;

(2) turning on the reset switches of all storage pixel sensors in the array for a reset period occurring during a first portion of said first time period and turning off said reset switches at the end of said first portion of said first time period;

(3) integrating photocurrent in all storage pixel sensors in the array for an integration period occurring during a second portion of said first time period after said reset switches have been turned off, said integration period ending at the end of said first time period;

(4) turning on the reset switches of all storage pixel sensors in the array for a reference period after the end of said first time period;

(5) selecting a row of the array and reading an output signal from each storage

pixel sensor in the selected row; and

(6) repeating step (5) until output signals for all storage pixel sensors in all rows of the array have been read.

22. A method for operating an array of storage pixel sensors of claim 1 arranged in rows, including the steps of:

- (1) turning on the transfer switches of all storage pixel sensors in the array for a first time period and turning off said transfer switches at the end of said first time period;
- (2) turning on the reset switches of all storage pixel sensors in the array for a reset period occurring during a first portion of said first time period and turning off said reset switches at the end of said first portion of said first time period;
- (3) integrating photocurrent in all storage pixel sensors in the array for an integration period occurring during a second portion of said first time period after said reset switches have been turned off, said integration period ending at the end of said first time period;
- (4) turning on the reset switches of all storage pixel sensors in the array for a reference period after the end of said first time period;
- (5) selecting a row of the array, reading an output signal from each storage pixel sensor in the selected row, then activating the transfer switches of all storage pixel sensors in the selected row and reading a reference signal from each storage pixel sensor in the selected row, then taking the difference between the output signal and the reference signal for each storage pixel sensor in the selected row; and
- (6) repeating step (5) until output signals and reference signals for all storage pixel sensors in all rows of the array have been read and correlated double sampled.

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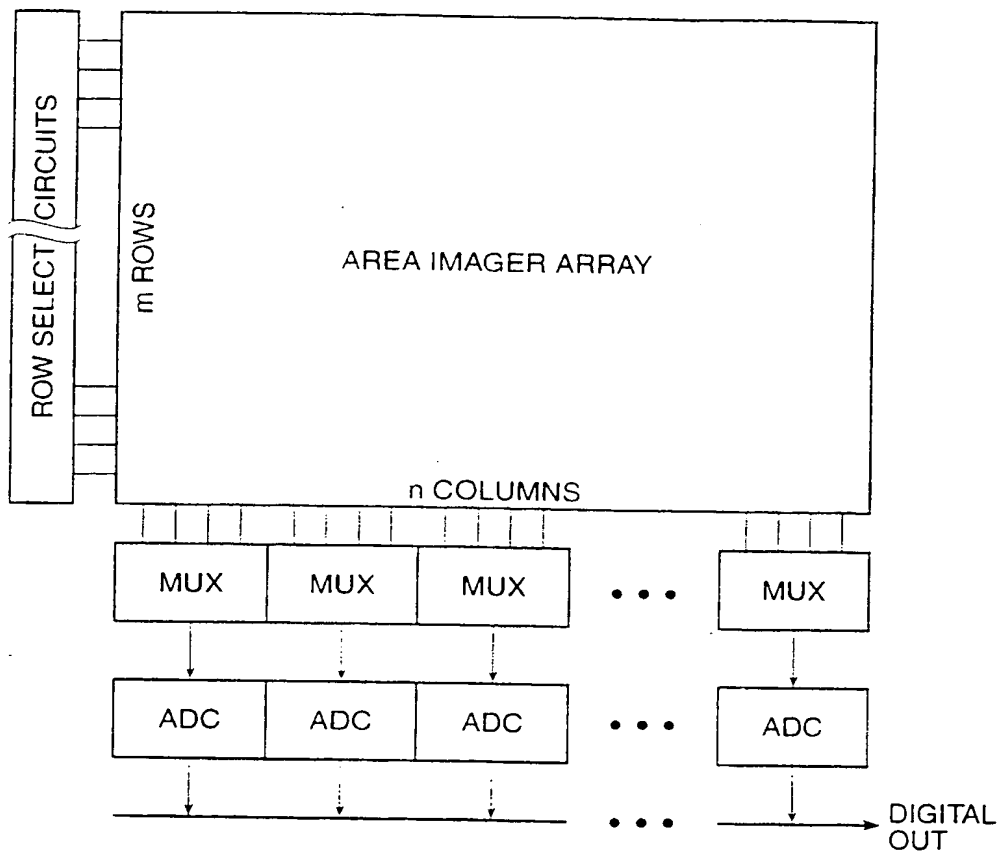


FIG. 1
(PRIOR ART)

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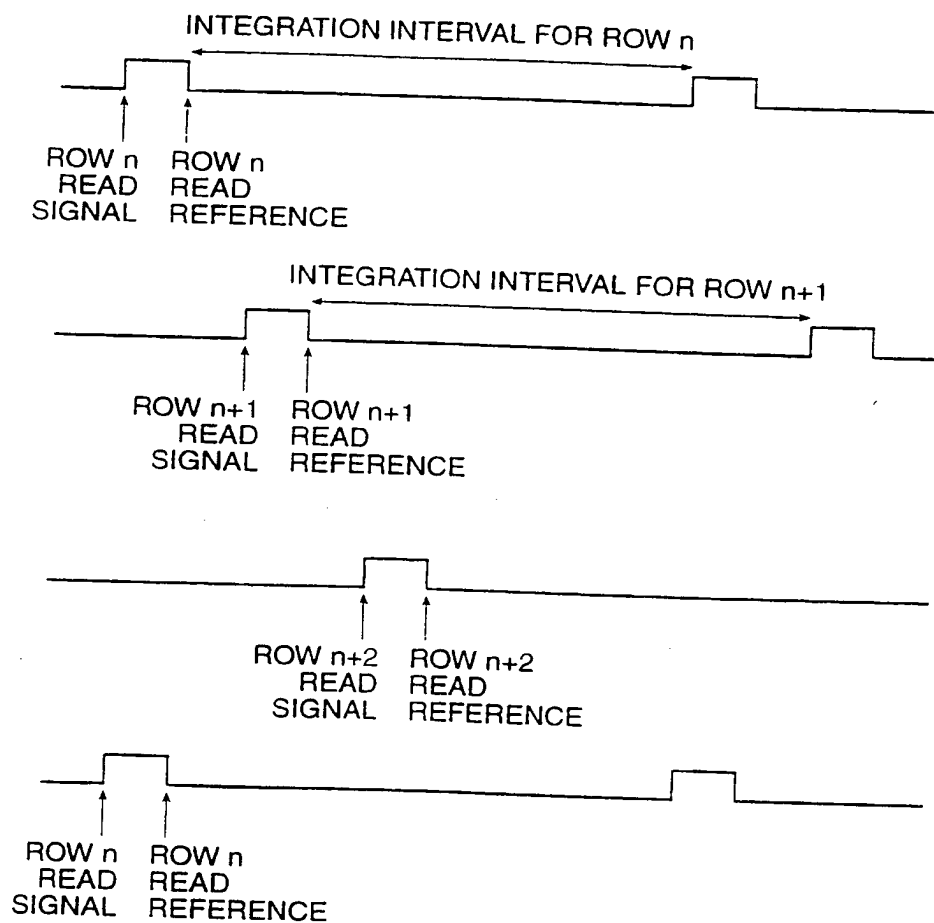


FIG. 2
(PRIOR ART)

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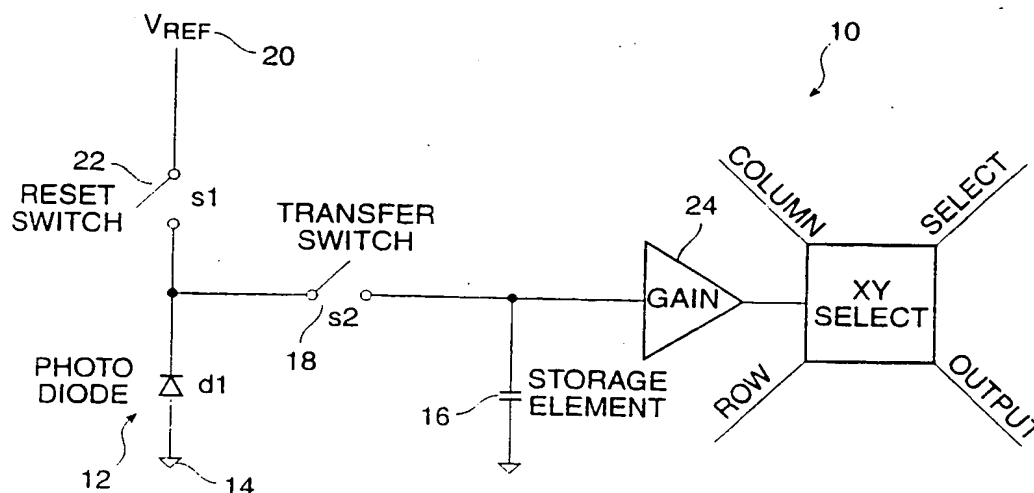


FIG. 3A

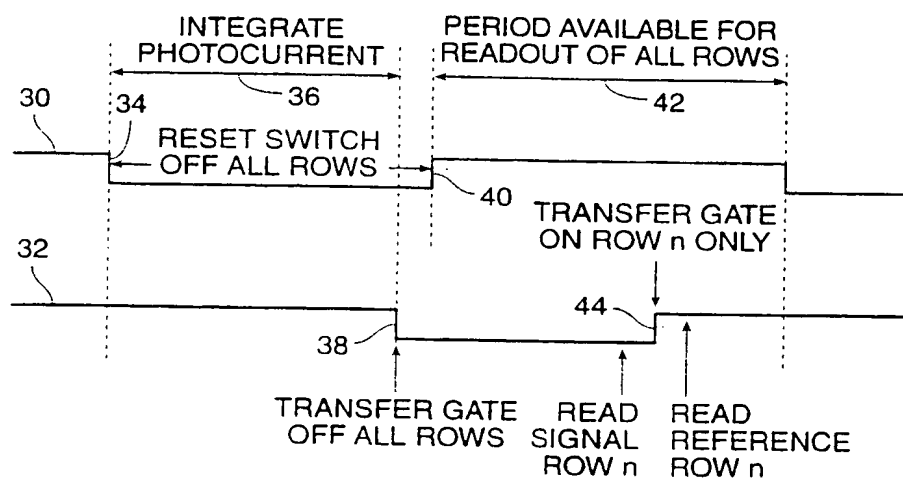


FIG. 3B

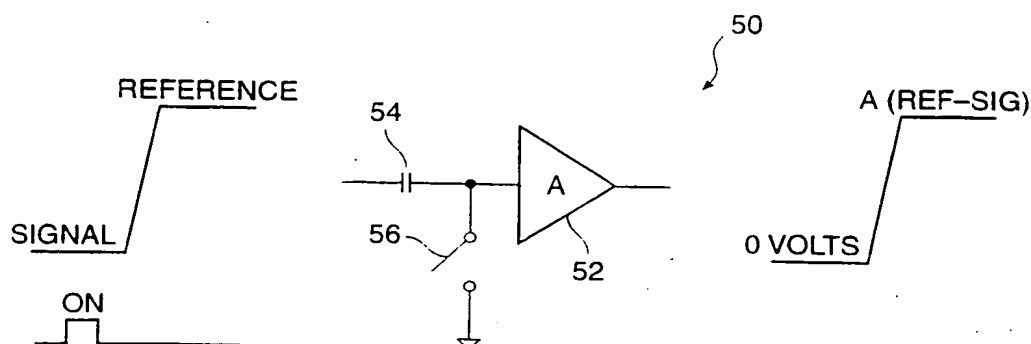


FIG. 4

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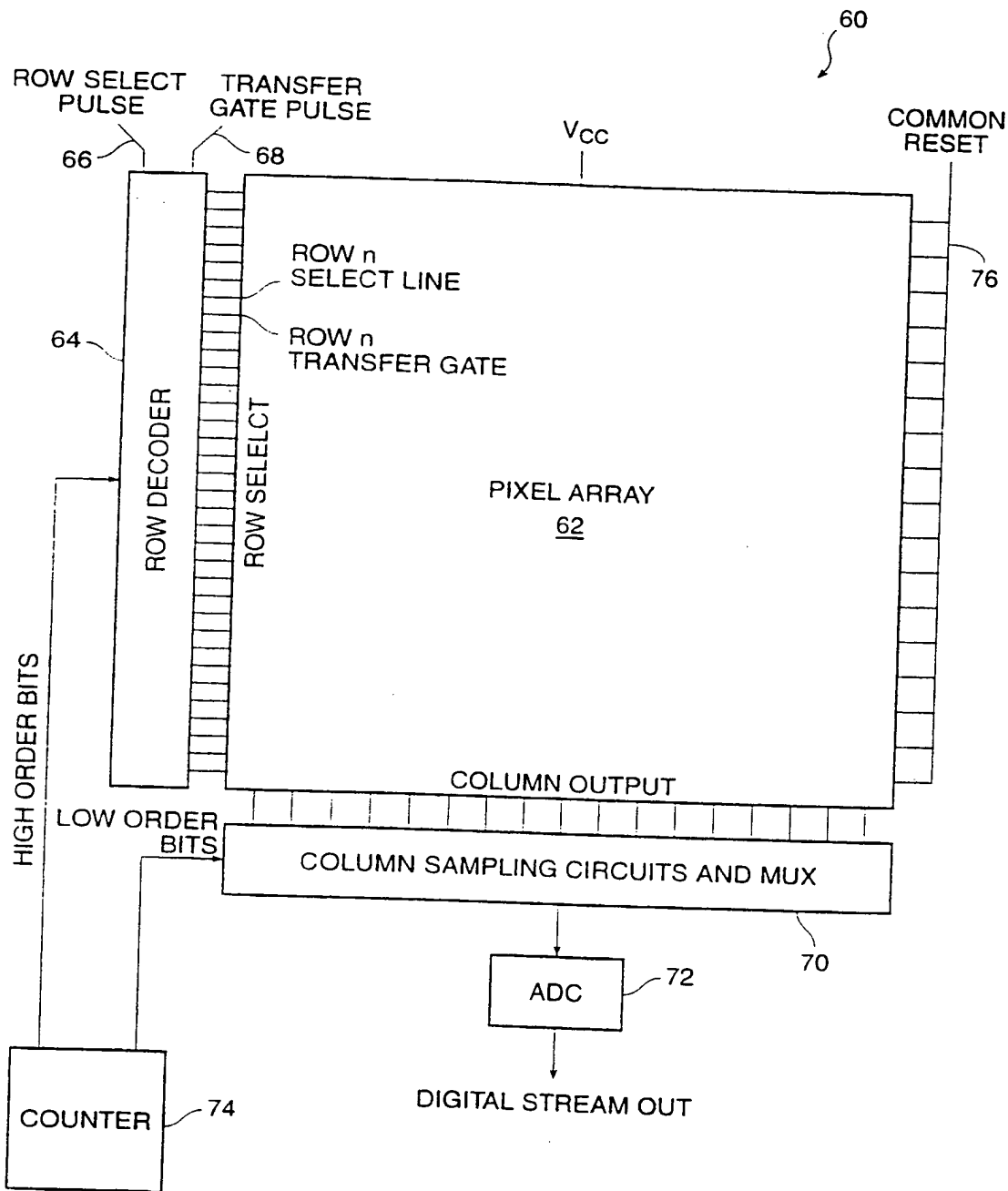


FIG. 5

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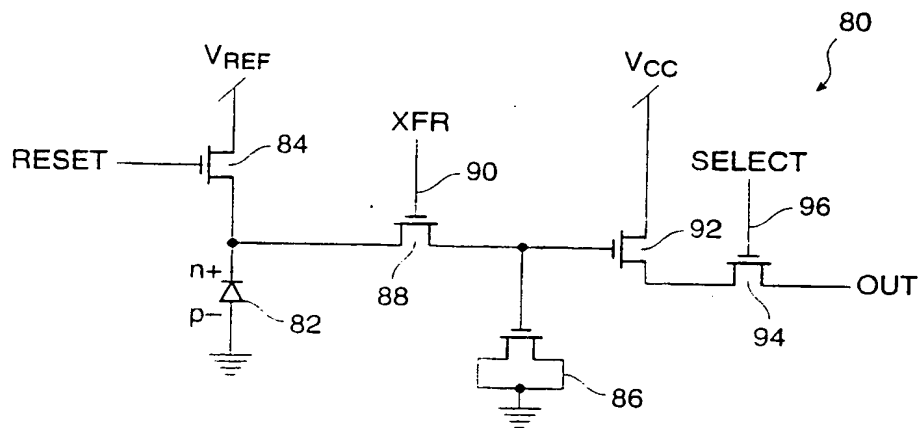


FIG. 6

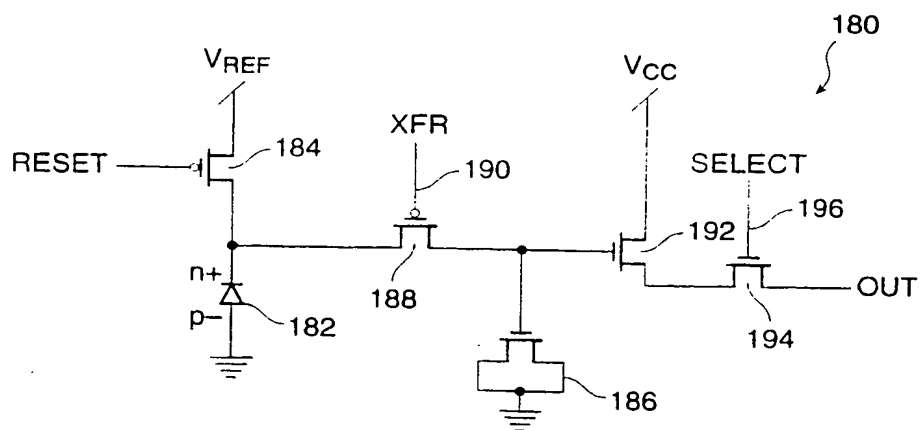


FIG. 8

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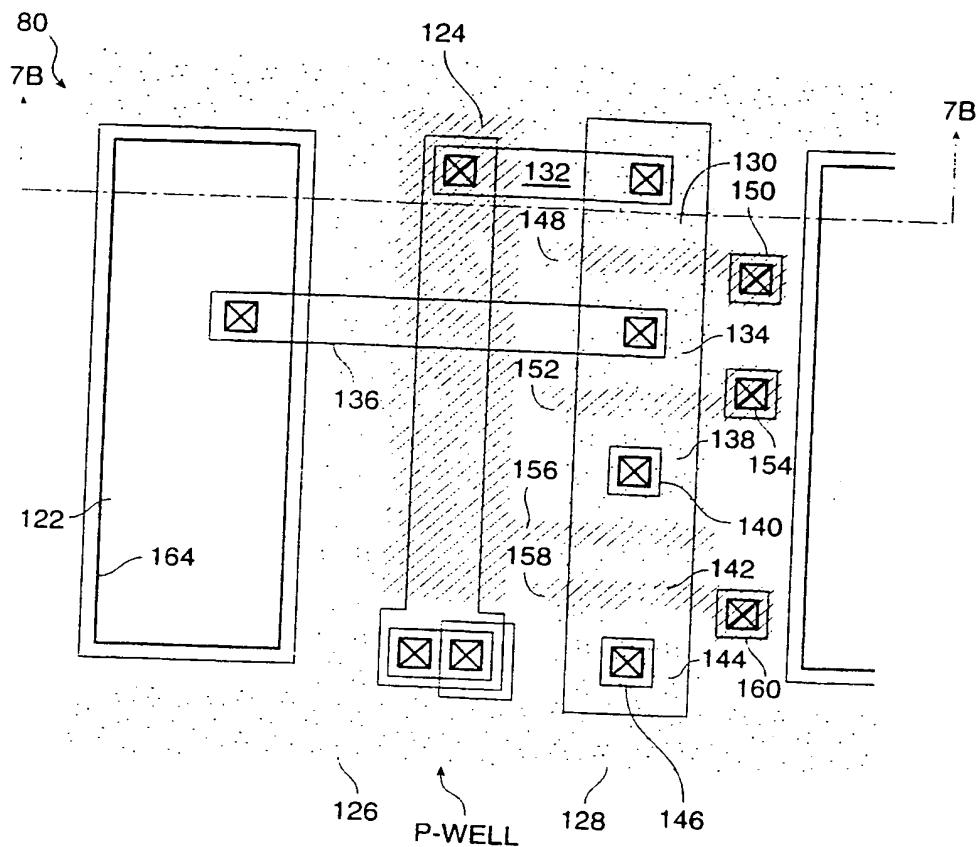


FIG. 7A

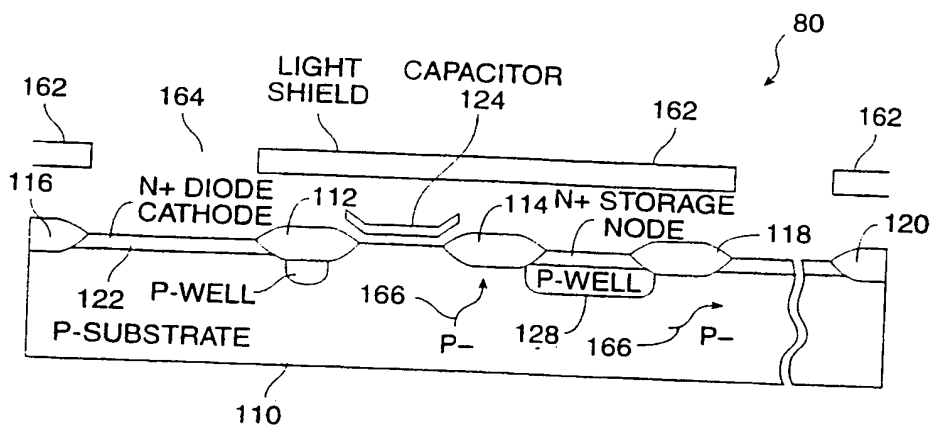


FIG. 7B

SUBSTITUTE SHEET (RULE 26)

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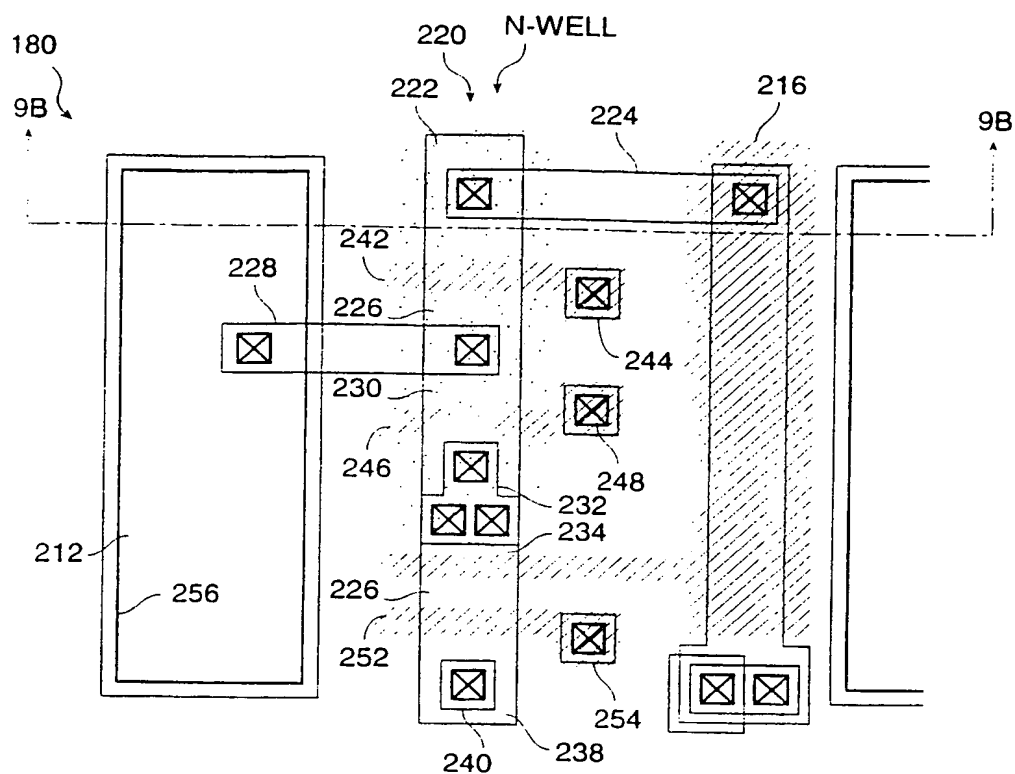


FIG. 9A

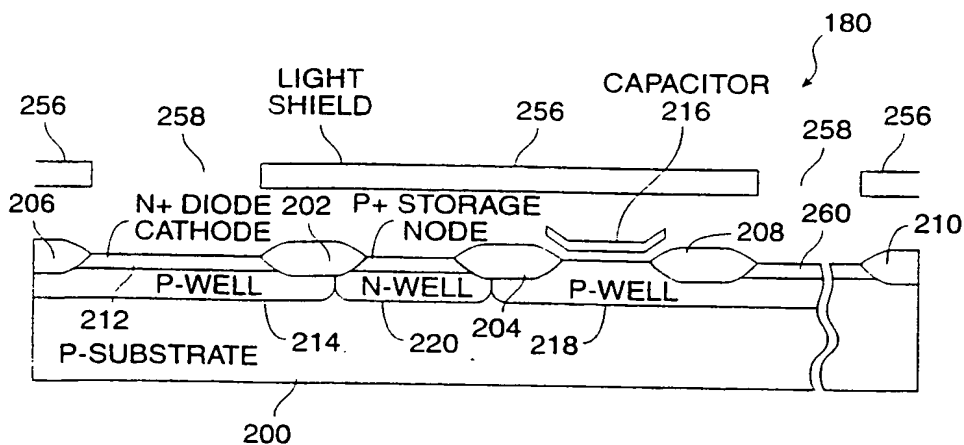


FIG. 9B

SUBSTITUTE SHEET (RULE 26)

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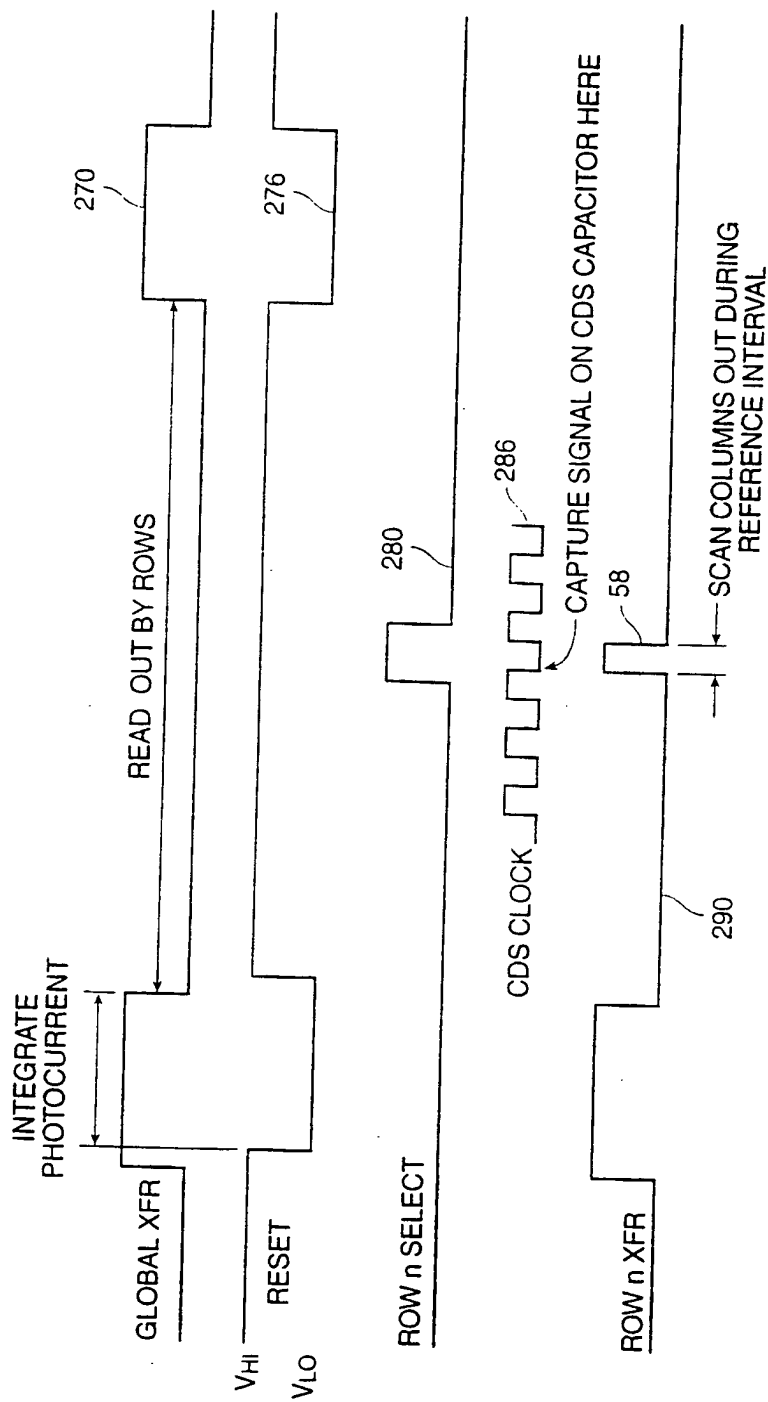


FIG. 10A

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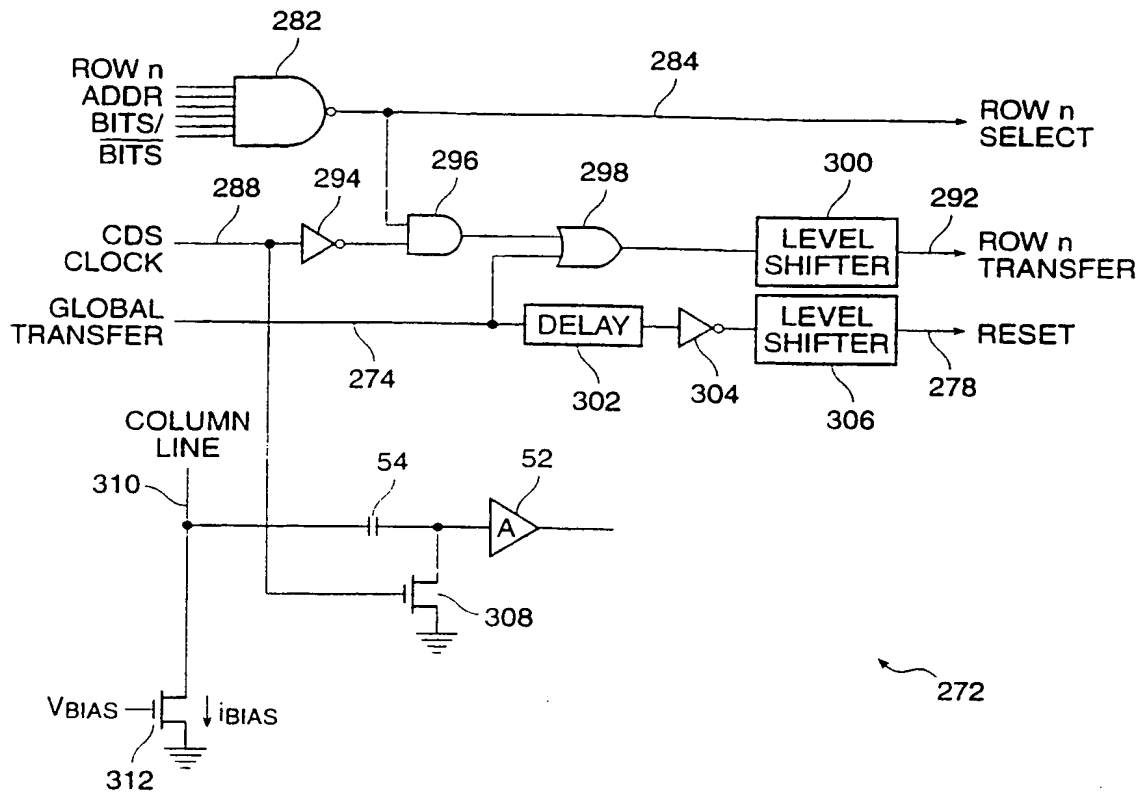


FIG. 10B

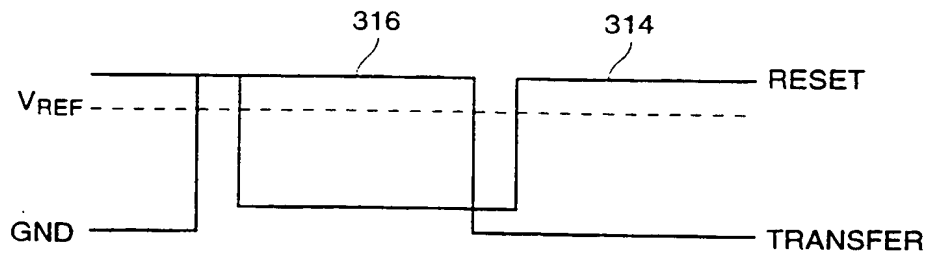


FIG. 11

INTERNATIONAL SEARCH REPORT

National Application No

/US 98/21692

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04N3/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CHYE HUAT AW ET AL: "A 128X128-PIXEL STANDARD-CMOS IMAGE SENSOR WITH ELECTRONIC SHUTTER" IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, vol. 39, February 1996, page 180/181, 440 XP000685586 see left-hand column, line 19 - line 56; figure 2	1,7,13, 19-22
X	US 4 839 735 A (KYOMASU MIKIO ET AL) 13 June 1989 see column 3, line 52 - column 4, line 37 see column 5, line 27 - line 44; figure 4	19-22
A	---	1,2,7,13
	-/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

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- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search

15 January 1999

Date of mailing of the international search report

22/01/1999

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Bequet, T

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 98/21692

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>EP 0 777 379 A (SGS THOMSON MICROELECTRONICS) 4 June 1997 see page 4, line 18 - line 32 see page 4, line 53 - line 55; table 1 -----</p>	<p>1, 7, 13, 19-22</p>

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/US 98/21692

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